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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/593,577	09/20/2006	Kiyoshi Kato	0756-7839	1460

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EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,577	KATO, KIYOSHI	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

NON-FINAL REJECTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/6/2008 has been entered.

Claims Rejections

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-28 are rejected under 35 USC 103 (a) as being unpatentable over Hirata (US 6,670,679) in view of Ueno et al (US 6,300,656).

Regarding claims 1-2 and 10, Hirata discloses in Figures 4 and 9-12A a circuit comprising:

- a transistor (104, 104a in Figure 10 or 60 in Figure 12A) having a floating gate (106, 106a in Figure 10 or 55 in Figure 12A) and a control gate (105, 105a in Figure 10 or 57 in Figure 12A), wherein the floating gate (55, Figure 12A) and the control gate (57) of the transistor (60) overlap each other with an insulating film (56, Figure 12A) interposed

therebetween; a drain or a source of the transistor is connected to the control gate; and the drain and the control gate are connected to an input terminal (32) and an output terminal, see Figure 10. Wherein the transistors (104, 104a) are thin film transistors.

However, Hirata does not disclose that a side surface of the floating gate is covered with a third insulation film, the floating gate is electrically floated and a plurality of transistors are connected in series so as to have the same forward current direction. For example, Figure 10 of Hirata shows each transistor (104) includes only one transistor and the floating gate (55) is coupled to ground through a resistor (RFG) for performing a pinch-off mode and uniform bipolar mode for protecting an internal circuit against the excessively high input voltage, see lines 25-40, column 4.

Nevertheless, Ueno et al suggests in Figure 1 a MOS transistor is formed with a floating gate (4), a control gate (6), insulating films (3, 5), and a third insulating film (7) covering sides surface of the floating gate (4), see lines 25-35, column 13, for reducing a longitudinal electric field at a point where a lateral electric field has a peak and the most hot electrons generate so as to increase a probability with which generated high energy electrons are injected into a floating gate electrode, see lines 58-65, column 4.

It would have been obvious to a person having skill in the art at the time the invention was made to form the MOS transistor of Hirata as suggested by Ueno et al for the purpose of reducing a longitudinal electric field at a point where a lateral electric field has a peak and the most hot electrons generate so as to increase a probability with which generated high energy electrons are injected into a floating gate electrode.

Also, a skilled artisan recognizes, as well known in the art, that the floating gate of a transistor can be connected to a predetermined bias voltage or can be electrically

floated and a series of diode connected transistors would increase voltage drops on these transistors. Thus, floating the floating gate of Hirata and employing a plurality of diode connected transistors as claimed is considered as a matter of a design expedient for an engineer depending upon the particular application in which the modified circuit of Hirata is to be used. It would have been obvious to a person having skill in the art at the time the invention was made to electrically float the float gate of Hirata and employ a plurality of diode connected transistors as claimed for the purpose of increasing voltage drops and accommodating with the requirement of a predetermined system.

Regarding claims 3-6, wherein the plurality of transistors (104, 104a) of Hirata are connected in series as shown in Figure 10.

Regarding claims 7 and 14-18, wherein the source/drain terminal of the transistor is connected to other lines so that it physically is connected to a connecting terminal or a connecting node, see Figures 10-12A.

Regarding claims 8, 13 and 19-23, since the resistor is a means for reducing current, a skilled artisan would have recognized that a resistor can be placed between the input and the drain of the transistor of Hirata for providing an over-current protection for this transistor. Thus, placing a resistor between the input and the drain terminal of the transistor of Hirata as claimed is considered to be a matter of a design expedient that would have been obvious at the time of the invention.

Regarding claims 10-12, since the circuit of Hirata is a protective circuit; obviously it may be used in a communication circuit comprising an antenna for protecting the communication circuit. Thus, employing the circuit of Hirata for protecting a predetermined communication circuit comprising an antenna is considered to be a matter

of a design expedient for an engineer that would have been obvious at the time of the invention.

Regarding claims 24-28, wherein the modified transistor of Hirata in view of Ueno et al is a thin film transistor.

Response to Applicant's

The Applicant argues that the floating gate electrode 55 of Hirata is connected to a source line or ground (see Figures 4-7 and 9-12) such that the floating gate is not electrically floating. The arguments are not persuasive because electrically floating the floating gate of Hirata is considered to be a matter of a design expedient for an engineer since, as well known in the art, the floating gate of a transistor can be biased by a predetermined voltage or floated depending upon a particular application that would have been obvious at the time of the invention.

The applicant argues that modifying Hirata with the floating gate electrodes 4 of Ueno would render Hirata unsatisfactory for its intended function of providing a protective circuit, as stated above, if doing so would potentially result in a floating gate that is "electrically floating." Therefore, the Applicant respectfully submits that Hirata, either alone or in combination with Ueno, does not teach or suggest a floating gate which is electrically floating and that the references cannot be combined in such a way as to teach all the claim imitations of the present invention. The arguments are not persuasive because the modified circuit of Hirata in view of Ueno would provide the structure of the claimed circuit as stated above. Thus, the modified circuit of Hirata would perform the

same function as the claimed circuit. Thus, the rejected claims remain readable on the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan, can be reached at (571) 272-1988.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/DINH T. LE/

Primary Examiner, Art Unit 2816